

**QUANTUM OPTICS LABORATORY**

ETH Zurich, Department of Physics  
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BACHELOR / SEMESTER / MASTER PROJECT – SPRING 2022:

**FPGA-based dual-camera readout for fast laser beam profiling**

**1. ADMINISTRATIVE DATA**

<b>Student</b>	-----;
<b>Affiliation (Section/semester)</b>	MSc Semester Project
<b>Project Schedule</b>	03.2022 through 6.2022
<b>Project Supervisors</b>	Philipp Fabritius, Dr. Abdulkadir Akin, Prof. Tilman Esslinger
<b>Project Delivery</b>	June 2022
<b>Contact Person</b>	fabritius@phys.ethz.ch, aakin@phys.ethz.ch

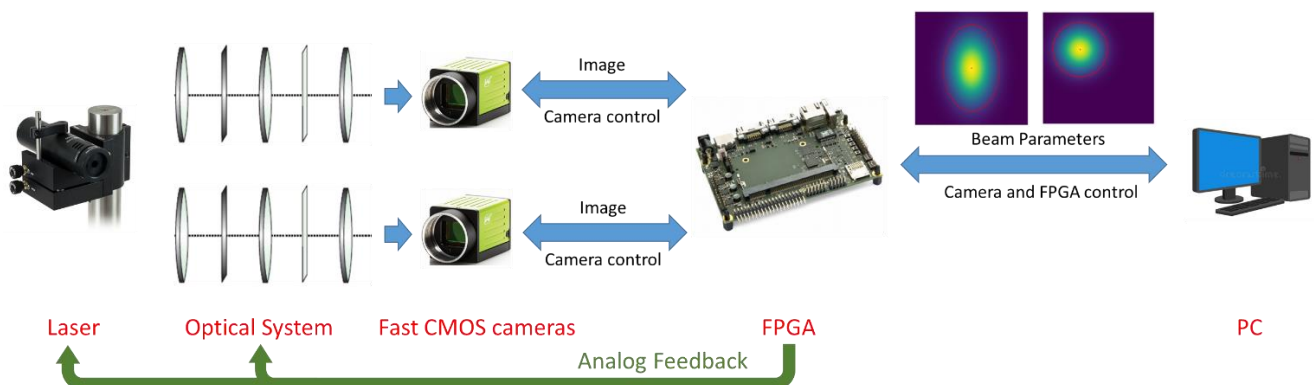
**2. PROJECT DEVELOPMENT AND FORESEEN MILESTONES**

Stable and well-defined laser beams are a base requirement for quantum experiments based on ultra-cold atoms in order to precisely control the physics. An FPGA- and two camera-based firmware that calculates the Gaussian parameters (center coordinate, width, azimuthal angle) of a laser beam was recently implemented at the Quantum Optics group. The current implementation doesn't perform any real-time interaction with a laser control electronics or the experiment. Therefore, it requires further improvements to make the system ready to use in quantum experiments and testing in the lab.

In order to reach this goal, you will implement a PID and DAC-based feedback loop between laser control and FPGA. You will increase the Ethernet-based communication throughput to send Gaussian parameters to PC as fast as the camera. You will integrate the Python-based FPGA control software into the experiment control software. Then you will test the system in an experiment.

The following further improvements would be performed with the availability of the time:

- Adjustable region of interest in the image
- Reducing FPGA-hardware resource utilization by resource-sharing technique
- Increasing the speed of width calculations



**Project Milestones:**

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|--|-------|
| • Study of the existing algorithm and digital image processing firmware    | (20%) |
| • Implementing PID loop for controlling laser with analog feedback         | (20%) |
| • Coding Python for PC and C for Zynq SoC for faster PC-FPGA communication | (20%) |
| • Integrating the system in Python-based experiment control setup          | (20%) |
| • Project report and presentation  | (20%) |

Signature: